## AMENDMENTS TO THE CLAIMS:

The listing of claims will replace all prior versions, and listings of claims in the application:

## LISTING OF THE CLAIMS

1. (Currently amended) A method of modifying a data model of an integrated circuit by electronic means, wherein the data model includes at least one layer of circuit components and wherein the method includes the steps of:

calculating a plurality of predetermined scaling ratios that include an interconnect scaling ratio including geometry width and spacing for each routing layer, a via size ratio in each via layer and a transistor geometry ratio;

selecting a scaling factor that is equal to or greater than the largest of the predetermined scaling ratios~~,~~;

scaling the entire circuit represented by the data model ~~according to~~ with the scaling factor~~,~~; and

adjusting each layer in the circuit for functionality and design rule compliance.

2. (Original) A method according to claim 1, wherein the electronic means includes a computer program arranged to run on a computer.



3. (Cancelled)

4. (Cancelled)

5. (Currently amended) A method according to claim ~~3~~1, wherein the data model of the integrated circuit includes a design grid and wherein the scaling factor is selected by rounding up to the next whole design grid point from the largest of the predetermined scaling ratios.

6. (Previously amended) A method according to claim 1, wherein the step of scaling the circuit according to the scaling factor includes multiplying the

coordinates of the circuit geometry by the scaling factor.

7. (Previously amended) A method according to claim 1, wherein the step of adjusting the circuit for functionality and design rule compliance includes a hierarchical layer scaling process whereby shapes in a sub-cell of the circuit may be scaled without breaking their connections with other parts of the circuit.

8. (Original) A method according to claim 7, wherein the hierarchical layer scaling process includes the step of identifying components that meet predetermined width criteria, and scaling only components that do not meet those criteria.

9. (Previously amended) A method according to claim 1, wherein the step of adjusting the circuit for functionality and design rule compliance includes a transistor edge adjustment process.

10. (Original) A method according to claim 9, wherein the transistor edge adjustment process includes the step of adjusting the width of the polysilicon layer and/or the length of the diffusion layer.

11. (Previously amended) A method according to claim 1, including the additional step of updating the contacts and vias by removing the existing contacts and vias and replacing them with new contacts and vias so as to reduce the current density through those contacts and vias.

12. (Previously amended) A method according to claim 1, including the step of adding and/or deleting layers in accordance with the target manufacturing process.

13. (Previously amended) A method according to claim 1, including the step of checking the circuit using a layout verification process.

14. (Previously amended) A method according to claim 1, including the

preliminary step of analyzing and modifying the circuit data.

15. (Currently amended) A method according to claim 1, including the step of adding ~~a~~ an information node containing design parameters to devices in the circuit.

16. (Cancelled)

17. (Cancelled)

18. (Cancelled)

19. (New) A method of modifying a data model of an integrated circuit by electronic means, wherein the data model includes at least one layer of circuit components and wherein the method includes the steps of:

selecting a scaling factor,

scaling the circuit represented by the data model with the scaling factor,

adjusting each layer in the circuit for functionality and design rule compliance, and

performing a transistor edge adjustment process.

20. (New) A method according to claim 19, wherein the electronic means includes a computer program arranged to run on a computer.

21. (New) A method according to claim 19, wherein the scaling factor is selected by calculating a plurality of predetermined scaling ratios and selecting a scaling factor that is equal to or greater than the largest of the predetermined scaling ratios.

22. (New) A method according to claim 21, wherein the predetermined scaling ratios include the interconnect scaling ratio including geometry width and spacing for each routing layer, the via size ratio in each via layer and the transistor geometry ratio.

23. (New) A method according to claim 19, wherein the data model of the integrated circuit includes a design grid and wherein the scaling factor is selected by rounding up to the next whole design grid point from the largest of the predetermined scaling ratios.

24. (New) A method according to claim 19, wherein the step of scaling the circuit according to the scaling factor includes multiplying the coordinates of the circuit geometry by the scaling factor.

25. (New) A method according to claim 19, wherein the step of adjusting the circuit for functionality and design rule compliance includes a hierarchical layer scaling process whereby shapes in a sub-cell of the circuit may be scaled without breaking their connections with other parts of the circuit.

26. (New) A method according to claim 25, wherein the hierarchical layer scaling process includes the step of identifying components that meet predetermined width criteria, and scaling only components that do not meet those criteria.

27. (New) A method according to claim 19, wherein the transistor edge adjustment process includes the step of adjusting the width of the polysilicon layer and/or the length of the diffusion layer.

28. (New) A method according to claim 19, including the additional step of updating the contacts and vias by removing the existing contacts and vias and replacing them with new contacts and vias so as to reduce the current density through those contacts and vias.

29. (New) A method according to claim 19, including the step of adding and/or deleting layers in accordance with the target manufacturing process.

30. (New) A method according to claim 19, including the step of checking

the circuit using a layout verification process.

31. (New) A method according to claim 19, including the preliminary step of analyzing and modifying the circuit data.

32. (New) A method according to claim 19, including the step of adding an information node containing design parameters to devices in the circuit.